LM4953 Boomer™ Audio Power Amplifier Series Ground-Referenced, Ultra Low Noise, Ceramic Speaker Driver

Check for Samples: LM4953, LM4953SDBD

FEATURES

- **Pop & Click Circuitry Eliminates Noise During Turn-On and Turn-Off Transitions**
- **Low, 1µA (Max) Shutdown Current**
- **Low, 7mA (Typ) Quiescent Current**
- **12.6Vpp Mono BTL Output, Load = 2µF+ 30Ω**
- **Thermal Shutdown**
- **Unity-Gain Stable**
- **External Gain Configuration Capability**

APPLICATIONS

- **Cellphone**
- **PDA**

KEY SPECIFICATIONS

- **Quiescent Power Supply Current (V_{dd} = 3V), 7mA(Typ)**
- **BTL Voltage Swing (2µF+30Ω load, 1% THD+N, V_{dd} = 3.6V), 12.6V_{pp} (Typ)**
- **Shutdown Current, 1µA (Max)**

DESCRIPTION

The LM4953 is an audio power amplifier designed for driving Ceramic Speaker in portable applications. When powered by a 3.6V supply, it is capable of forcing 12.6Vpp across a 2µF + 30Ω bridge-tied-load (BTL) with less than 1% THD+N.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4953 does not require bootstrap capacitors, or snubber circuits. Therefore it is ideally suited for display applications requiring high power and minimal size.

The LM4953 features a low-power consumption shutdown mode. Additionally, the LM4953 features an internal thermal shutdown protection mechanism.

The LM4953 contains advanced pop & click circuitry that eliminates noises which would otherwise occur during turn-on and turn-off transitions.

The LM4953 is unity-gain stable and can be configured by external gain-setting resistors.

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Typical Application

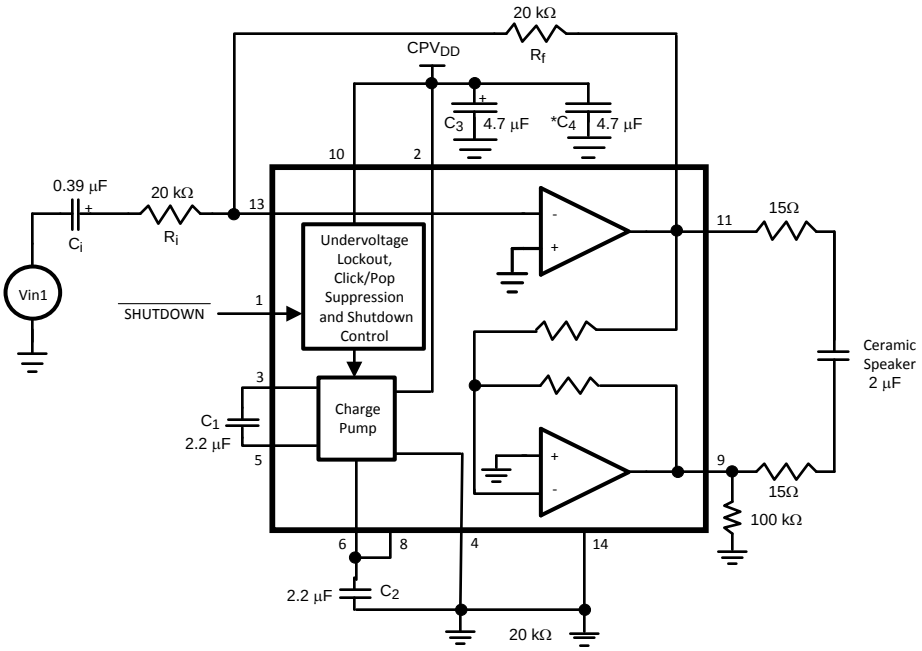

Figure 1. Typical Application Circuit

Connection Diagram

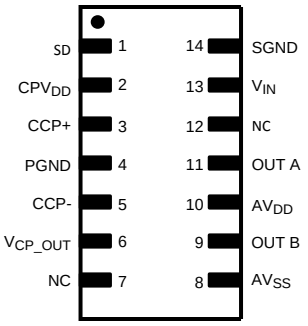

Figure 2. WSON Package
Top View
See Package Number NHK0014A

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PIN DESCRIPTIONS

Pin	Name	Function
1	SD	Active Low Shutdown
2	CP_{VDD}	Charge Pump Power Supply
3	CCP+	Positive Terminal - Charge Pump Flying Capacitor
4	PGND	Power Ground
5	CCP-	Negative Terminal - Charge Pump Flying Capacitor
6	V_{CP_OUT}	Charge Pump Output
7	NC	No Connect
8	AV_{SS}	Negative Power Supply - Amplifier
9	OUT B	Output B
10	AV_{DD}	Positive Power Supply - Amplifier
11	OUT A	Output A
12	NC	No Connect
13	V_{IN}	Signal Input
14	SGND	Signal Ground

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[(1)(2)(3)]

Supply Voltage (V_{DD})	4.5V
Storage Temperature	−65°C to +150°C
Input Voltage	-0.3V to V_{DD} + 0.3V
Power Dissipation[(4)]	Internally Limited
ESD Susceptibility[(5)(6)]	2000V
ESD Susceptibility[(7)(6)]	200V
Junction Temperature	150°C
Thermal Resistance	
See AN-1187(SNOA401) 'Leadless Leadframe Packaging (LLP).'	

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions that ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given; however, the typical value is a good indication of device performance.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} – T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4xxx typical application (shown in Figure 1) with V_{DD} = yyV, R_L = 2µF+30Ω mono BTL operation the total power dissipation is xxxW. θ_{JA} = 40°C/W.
(5) Human body model, 100pF discharged through a 1.5kΩ resistor.
(6) If the product is in shutdown mode and V_{DD} exceeds 3.6V (to a max of 4V V_{DD}), then most of the excess current will flow through the ESD protection circuits. If the source impedance limits the current to a max of 10mA, then the part will be protected. If the part is enabled when V_{DD} is above 4V, circuit performance will be curtailed or the part may be permanently damaged.
(7) Machine Model, 220pF-240pF discharged through all pins.

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	−40°C ≤ T_A ≤ 85°C
Supply Voltage (V_{DD})		1.6V ≤ V_{DD} ≤ 4.2V

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Electrical Characteristics V_{DD} = 3.6V

The following specifications apply for V_{DD} = 3.6V, $A_{V\text{-}BTL}$ = 6dB, Z_L = 2µF+30Ω unless otherwise specified. Limits apply to T_A = 25°C. See Figure 1.

Symbol	Parameter	Conditions	LM4953		Units (Limits)
			Typ(1)	Limit(2)(3)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0, R_{LOAD} = 2µF+30Ω	8		mA (max)
$I_{standby}$	Quiescent Power Supply Current Auto Standby Mode	V_{IN} = 0, Z_{LOAD} = 2µF+30Ω	2.7		mA
I_{SD}	Shutdown Current	V_{SD} = GND	0.1	1	µA (max)
V_{SDIH}	Shutdown Voltage Input High	SD1 SD2		0.7*CPVdd	V (min)
V_{SDIL}	Shutdown Voltage Input Low	SD1 SD2		0.3*CPVdd	V (max)
T_{WU}	Wake-up Time		125		µsec
V_{OS}	Output Offset Voltage		1	10	mV (max)
V_{OUT}	Output Voltage Swing	THD = 1% (max); f = 1kHz R_L = 2µF+30Ω, Mono BTL	12.6		Vpp
THD+N	Total Harmonic Distortion + Noise	V_{OUT} = 6Vp-p, f_{IN} = 1kHz	0.02		%
ϵ_{OS}	Output Noise	A-Weighted Filter, V_{IN} = 0V	15		µV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mVp-p, f = 217Hz, Input Referred	67		dB
		V_{RIPPLE} = 200mVp-p, f = 1kHz, Input Referred	65		dB
SNR	Signal-to-Noise Ratio	Z_L = 2µF+30Ω, V_{OUT} = 6Vp-p	105		dB

(1) Typicals are measured at 25°C and represent the parametric norm.
(2) Limits are specified to Texas Instruments' AOQL (Average Outgoing Quality Level).
(3) Datasheet min/max specification limits are specified by design, test, or statistical analysis.

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Electrical Characteristics V_{DD} = 3.0V

The following specifications apply for V_{DD} = 3.0V, $A_{V\text{-}BTL}$ = 6dB, Z_L = 2µF+30Ω unless otherwise specified. Limits apply to T_A = 25°C. See Figure 1.

Symbol	Parameter	Conditions	LM4953		Units (Limits)
			Typ(1)	Limit(2)(3)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0, Z_{LOAD} = 2µF+30Ω	7	10	mA (max)
$I_{standby}$	Quiescent Power Supply Current Auto Standby Mode	V_{IN} = 0, Z_{LOAD} = 2µF+30Ω	2.3		mA
I_{SD}	Shutdown Current	$V_{SD\text{-}LC}$ = $V_{SD\text{-}RC}$ = GND	0.1	1	µA (max)
V_{SDIH}	Shutdown Voltage Input High	SD1 SD2		0.7*CPVdd	V (min)
V_{SDIL}	Shutdown Voltage Input Low	SD1 SD2		0.3*CPVdd	V (max)
T_{WU}	Wake-up Time		125		µsec
V_{OS}	Output Offset Voltage		1	10	mV (max)
V_{OUT}	Output Voltage Swing	THD = 1% (max); f = 1kHz Z_L = 2µF+30Ω, Mono BTL	10.2		Vpp
THD+N	Total Harmonic Distortion + Noise	V_{OUT} = 8.5Vp-p, f_{IN} = 1kHz	0.02		%
ϵ_{OS}	Output Noise	A-Weighted Filter, V_{IN} = 0V	15		µV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mVp-p, f = 217Hz, Input Referred	73		dB
		V_{RIPPLE} = 200mVp-p, f = 1kHz, Input Referred	68		dB
SNR	Signal-to-Noise Ratio	Z_L = 2µF+30Ω, V_{OUT} = 8.5Vp-p	105		dB

(1) Typicals are measured at 25°C and represent the parametric norm.
(2) Limits are specified to Texas Instruments' AOQL (Average Outgoing Quality Level).
(3) Datasheet min/max specification limits are specified by design, test, or statistical analysis.

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Typical Performance Characteristics

THD+N vs Frequency
V_{DD} = 2V, V_O = 2Vpp, Z_L = 2µF+30Ω

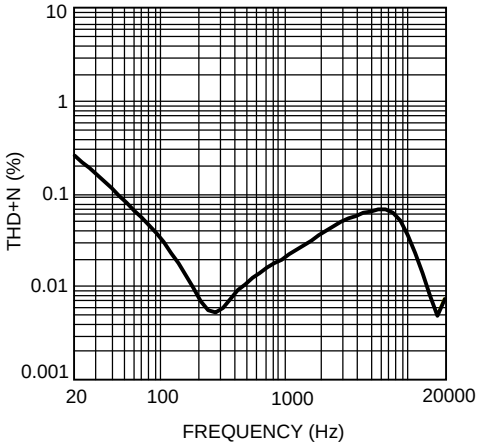

Figure 3.

THD+N vs Frequency
V_{DD} = 3V, V_O = 6Vpp, Z_L = 2µF+30Ω

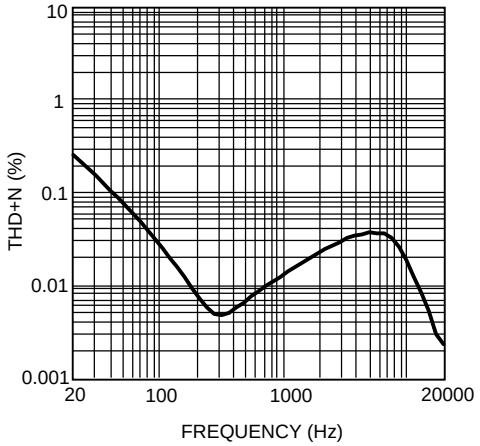

Figure 4.

THD+N vs Frequency
V_{DD} = 3.6V, V_O = 8.5Vpp, Z_L = 2µF+30Ω

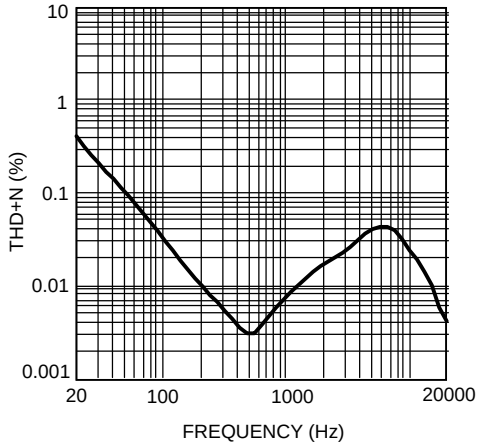

Figure 5.

THD+N vs Frequency
V_{DD} = 4.2V, V_O = 10Vpp, Z_L = 2µF+30Ω

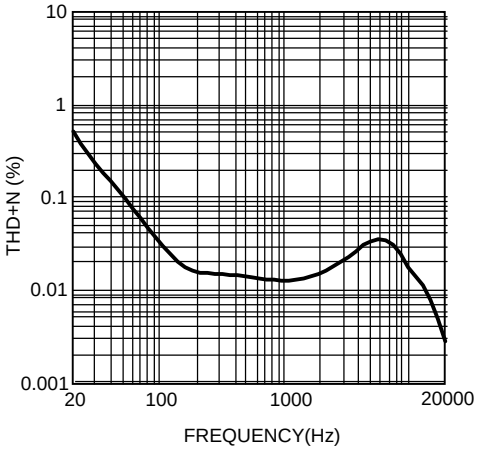

Figure 6.

THD+N vs Output Voltage
V_{DD} = 2V, f = 1kHz, Z_L = 2µF+30Ω

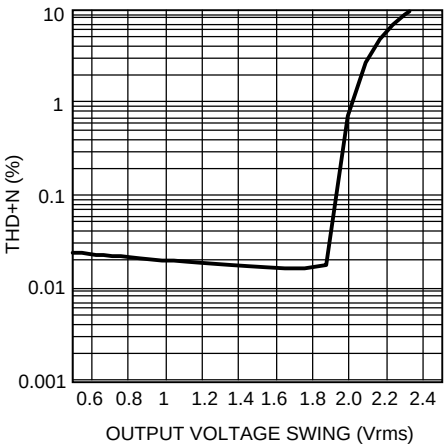

Figure 7.

THD+N vs Output Voltage
V_{DD} = 3V, f = 1kHz, Z_L = 2µF+30Ω

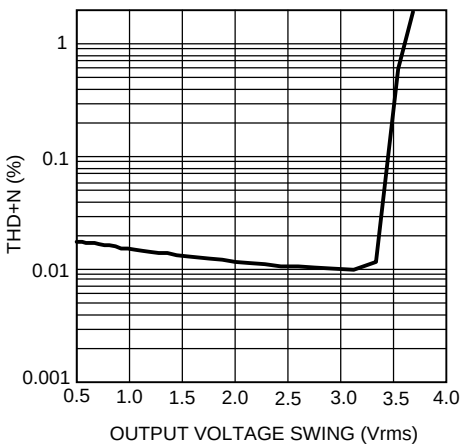

Figure 8.

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Typical Performance Characteristics (continued)

THD+N vs Output Voltage
V_{DD} = 3.6V, f = 1kHz, Z_L = 2µF+30Ω

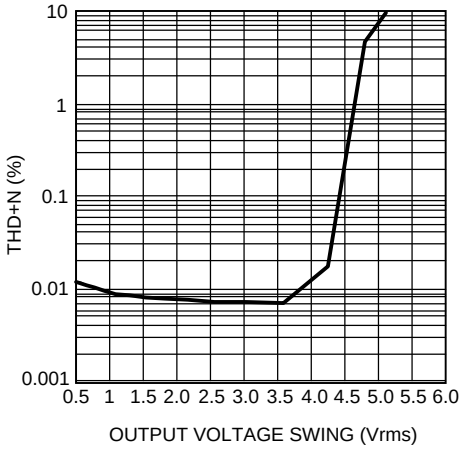

Figure 9.

THD+N vs Output Voltage
V_{DD} = 4.2V, f = 1kHz, Z_L = 2µF+30Ω

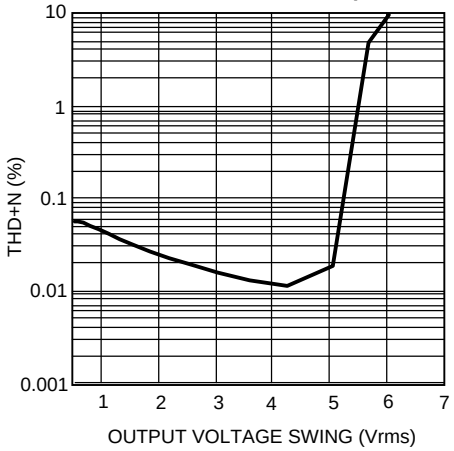

Figure 10.

PSRR vs Frequency
V_{DD} = 2V, Z_L = 2µF+30Ω

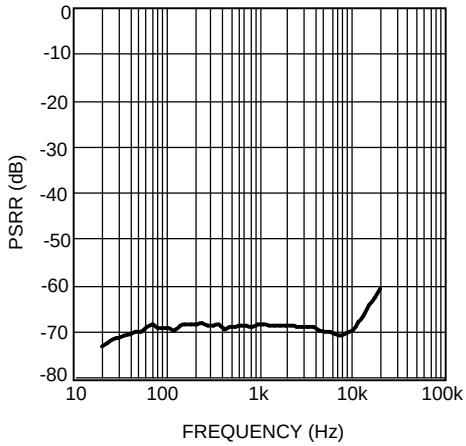

Figure 11.

PSRR vs Frequency
V_{DD} = 3V, Z_L = 2µF+30Ω

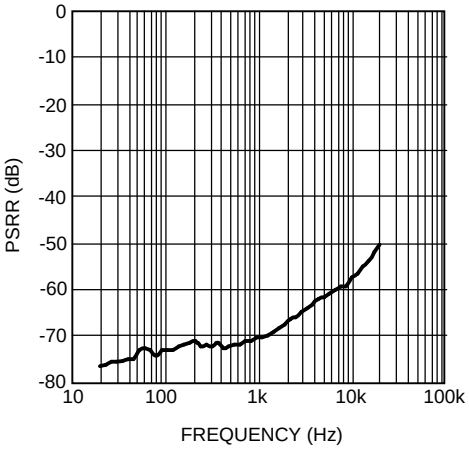

Figure 12.

PSRR vs Frequency
V_{DD} = 3.6V, Z_L = 2µF+30Ω

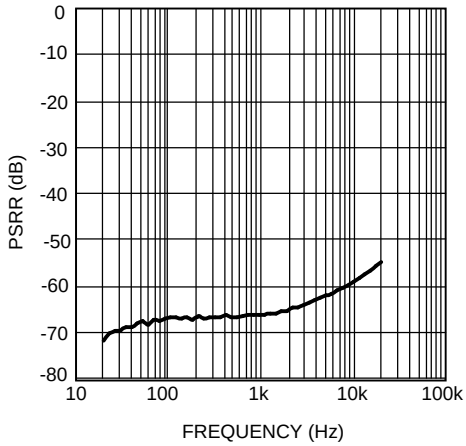

Figure 13.

PSRR vs Frequency
V_{DD} = 4.2V, Z_L = 2µF+30Ω

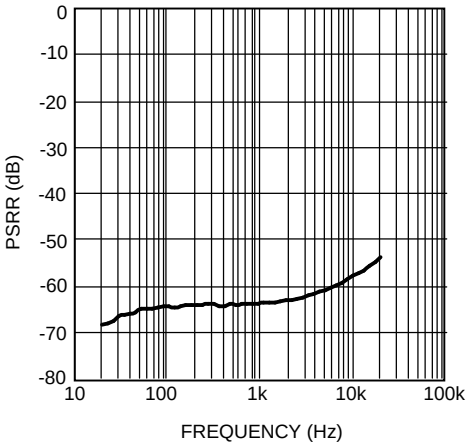

Figure 14.

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Typical Performance Characteristics (continued)

Supply Current vs Supply Voltage
Z_L = 2µF+30Ω

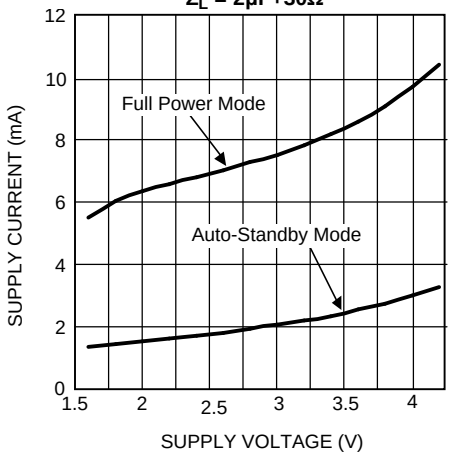

Figure 15.

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APPLICATION INFORMATION

ELIMINATING THE OUTPUT COUPLING CAPACITOR

The LM4953 features a low noise inverting charge pump that generates an internal negative supply voltage. This allows the outputs of the LM4953 to be biased about GND instead of a nominal DC voltage, like traditional headphone amplifiers. Because there is no DC component, the large DC blocking capacitors (typically 220µF) are not necessary. The coupling capacitors are replaced by two, small ceramic charge pump capacitors, saving board space and cost.

Eliminating the output coupling capacitors also improves low frequency response. In traditional headphone amplifiers, the headphone impedance and the output capacitor form a high pass filter that not only blocks the DC component of the output, but also attenuates low frequencies, impacting the bass response. Because the LM4953 does not require the output coupling capacitors, the low frequency response of the device is not degraded by external components.

In addition to eliminating the output coupling capacitors, the ground referenced output nearly doubles the available dynamic range of the LM4953 when compared to a traditional headphone amplifier operating from the same supply voltage.

BRIDGE CONFIGURATION EXPLANATION

The Audio Amplifier portion of the LM4953has two internal amplifiers allowing different amplifier configurations. The first amplifier's gain is externally configurable, whereas the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of Rf to Ri while the second amplifier's gain is fixed by the two internal 20kΩ resistors. Figure 1 shows that the output of amplifier one serves as the input to amplifier two. This results in both amplifiers producing signals identical in magnitude, but out of phase by 180°. Consequently, the differential gain for the Audio Amplifier is

$$A_{VD} = 2 *(Rf/Ri) \quad (1)$$

By driving the load differentially through outputs OUT A and OUT B, an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classic single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration. It provides differential drive to the load, thus doubling the output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the **Audio Power Amplifier Design** section.

The bridge configuration also creates a second advantage over single-ended amplifiers. Since the differential outputs, OUT A and OUT B, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

OUTPUT TRANSIENT ('CLICK AND POPS') ELIMINATED

The LM4953 contains advanced circuitry that virtually eliminates output transients ('clicks and pops'). This circuitry prevents all traces of transients when the supply voltage is first applied or when the part resumes operation after coming out of shutdown mode.

POWER DISSIPATION

Power dissipation is a major concern when using any power amplifier and must be thoroughly understood to ensure a successful design. Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 Z_L) \quad (2)$$

Since the LM4953 has two operational amplifiers in one package, the maximum internal power dissipation point is twice that of the number which results from Equation 2. Even with large internal power dissipation, the LM4953 does not require heat sinking over a large range of ambient temperatures. The maximum power dissipation point obtained must not be greater than the power dissipation that results from Equation 3:

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$$P_{DMAX} = (T_{JMAX} - T_A) / (\theta_{JA}) \quad (3)$$

Depending on the ambient temperature, T_A, of the system surroundings, Equation 3 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 2 is greater than that of Equation 3, then either the supply voltage must be decreased, the load impedance increased or T_A reduced. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature may be increased accordingly.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 3V power supply typically use a 4.7µF capacitor in parallel with a 0.1µF ceramic filter capacitor to stabilize the power supply's output, reduce noise on the supply line, and improve the supply's transient response. Keep the length of leads and traces that connect capacitors between the LM4953's power supply pin and ground as short as possible.

AUTOMATIC STANDBY MODE

The LM4953 features Automatic Standby Mode circuitry (patent pending). In the absence of an input signal, after approximately 3 seconds, the LM4953 goes into low current standby mode. The LM4953 recovers into full power operating mode immediately after a signal, which is greater than the input threshold voltage, is applied to either the left or right input pins. The input threshold voltage is not a static value, as the supply voltage increases, the input threshold voltage decreases. This feature reduces power supply current consumption in battery operated applications.

To ensure correct operation of Automatic Standby Mode, proper layout techniques should be implemented. Separating PGND and SGND can help reduce noise entering the LM4953 in noisy environments. It is also important to use correct power off sequencing. The device should be in shutdown and then powered off in order to ensure proper functionality of the Auto-Standby feature. While Automatic Standby Mode reduces power consumption very effectively during silent periods, maximum power saving is achieved by putting the device into shutdown when it is not in use.

MICRO POWER SHUTDOWN

The voltage applied to the $\overline{SD}$ controls the LM4953's shutdown function. When active, the LM4953's micropower shutdown feature turns off the amplifiers' bias circuitry, reducing the supply current. The trigger point is $0.3*CPV_{DD}$ for a logic-low level, and $0.7*CPV_{DD}$ for logic-high level. The low 0.01µA (typ) shutdown current is achieved by applying a voltage that is as near as ground a possible to the $\overline{SD}$ pins. A voltage that is higher than ground may increase the shutdown current.

There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 100kΩ pull-up resistor between the $\overline{SD}$ pins and V_{DD}. Connect the switch between the $\overline{SD}$ pins and ground. Select normal amplifier operation by opening the switch. Closing the switch connects the $\overline{SD}$ pins to ground, activating micro-power shutdown. The switch and resistor ensure that the $\overline{SD}$ pins will not float. This prevents unwanted state changes. In a system with a microprocessor or microcontroller, use a digital output to apply the control voltage to the $\overline{SD}$ pins. Driving the $\overline{SD}$ pins with active circuitry eliminates the pull-up resistor.

EXPOSED-DAP CONSIDERATIONS

It is essential that the exposed Die Attach Paddle (DAP), for the LM4953, is NOT connected to GND. For optimal operation it should be connected to AVss and VCP-OUT (Pins 6 and 8).

SELECTING PROPER EXTERNAL COMPONENTS

Optimizing the LM4953's performance requires properly selecting external components. Though the LM4953 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

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Charge Pump Capacitor Selection

Use low ESR (equivalent series resistance) (<100mΩ) ceramic capacitors with an X7R dielectric for best performance. Low ESR capacitors keep the charge pump output impedance to a minimum, extending the headroom on the negative supply. Higher ESR capacitors result in reduced output power from the audio amplifiers.

Charge pump load regulation and output impedance are affected by the value of the flying capacitor (C1). A larger valued C1 (up to 3.3uF) improves load regulation and minimizes charge pump output resistance. Beyond 3.3uF, the switch-on resistance dominates the output impedance for capacitor values above 2.2uF.

The output ripple is affected by the value and ESR of the output capacitor (C2). Larger capacitors reduce output ripple on the negative power supply. Lower ESR capacitors minimize the output ripple and reduce the output impedance of the charge pump.

The LM4953 charge pump design is optimized for 2.2uF, low ESR, ceramic, flying, and output capacitors.

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitors (C_i in Figure 1). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using high value input and output capacitors.

Besides affecting system cost and size, C_i has an effect on the LM4953's click and pop performance. The magnitude of the pop is directly proportional to the input capacitor's size. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired −3dB frequency.

As shown in Figure 1, the internal input resistor, R_i and the input capacitor, C_i, produce a -3dB high pass filter cutoff frequency that is found using Equation 4. Conventional headphone amplifiers require output capacitors; Equation 4 can be used, along with the value of R_L, to determine towards the value of output capacitor needed to produce a –3dB high pass filter cutoff frequency.

$$f_{i\text{-}3dB} = 1 / 2\pi R_i C_i \quad (4)$$

Also, careful consideration must be taken in selecting a certain type of capacitor to be used in the system. Different types of capacitors (tantalum, electrolytic, ceramic) have unique performance characteristics and may affect overall system performance. (See the section entitled Charge Pump Capacitor Selection.)

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LM4953 DEMO BOARD ARTWORK

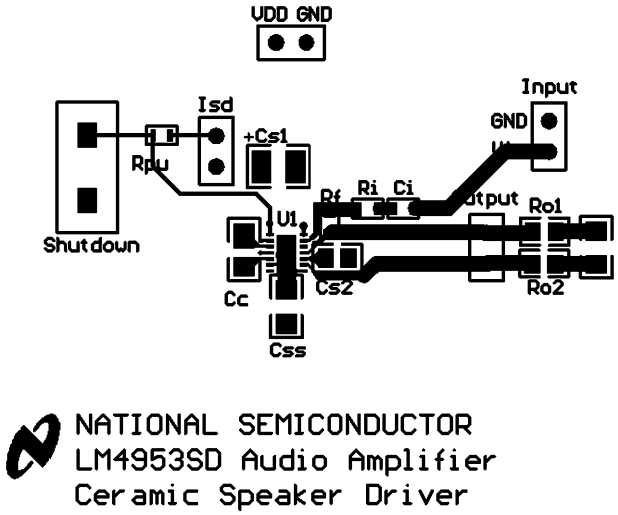

Figure 16. Top Layer

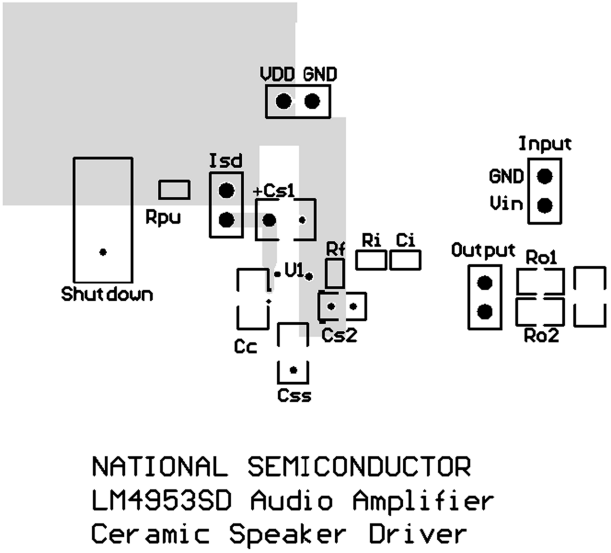

Figure 17. Mid Layer 1

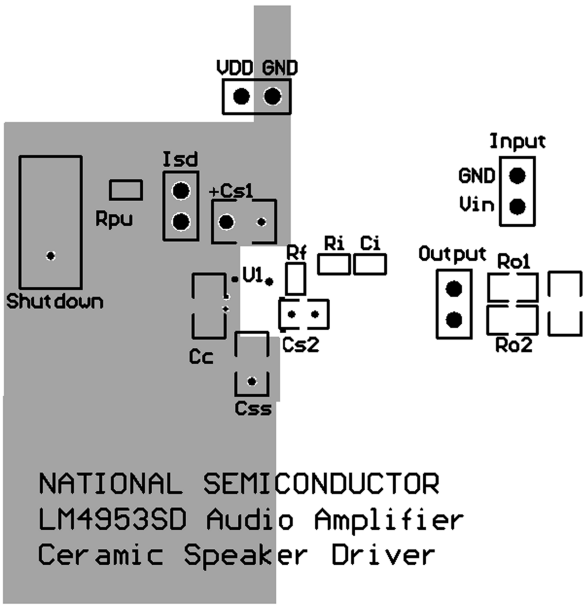

Figure 18. Mid Layer 2

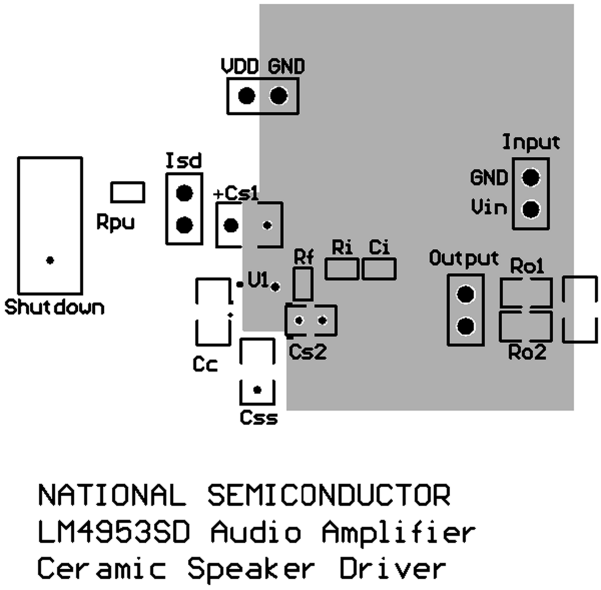

Figure 19. Bottom Layer

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REVISION HISTORY

Rev	Date	Description
1.0	2/18/05	Started D/S by copying LM4926 (DS201161).
1.2	9/13/05	Added the Typ Perf curves and Application Info section.
1.3	9/14/05	Added more Typ Perf curves. First WEB release on the D/S.
1.4	9/19/05	Fixed some typo, then re-released D/S to the WEB.
1.5	11/11/05	Added the WSON boards, then re-released D/S to the WEB... not released on this date..
1.6	11/14/05	Added the WSON boards, then re-released D/S to the WEB (per Nisha).
1.7	11/15/05	Text edit.
1.8	12/21/05	Added the EXPOSED-DAP CONSIDERATIONS (Application Info section), then re-released D/S to the WEB.
1.9	2/01/06	Edited 20142168 (Typ Appl ckt)..., then re-released D/S to the WEB.

Changes from Revision E (April 2013) to Revision F **Page**

- Changed layout of National Data Sheet to TI format 12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM4953SD/NOPB	ACTIVE	WSON	NHK	14	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L4953	Samples
LM4953SDX/NOPB	ACTIVE	WSON	NHK	14	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L4953	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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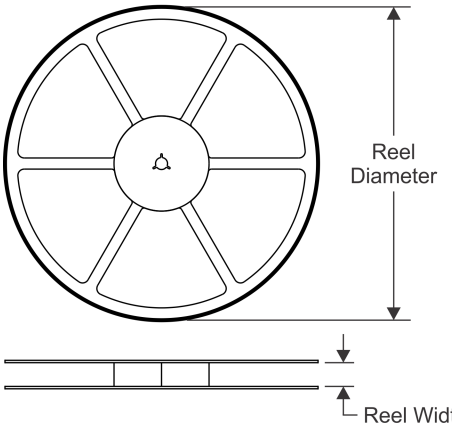
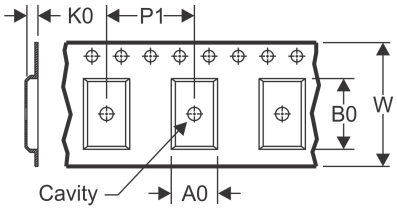
TAPE AND REEL INFORMATION

REEL DIMENSIONS

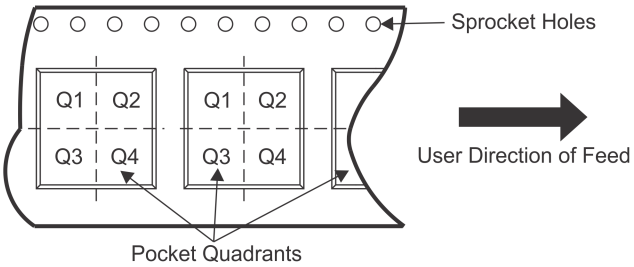


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

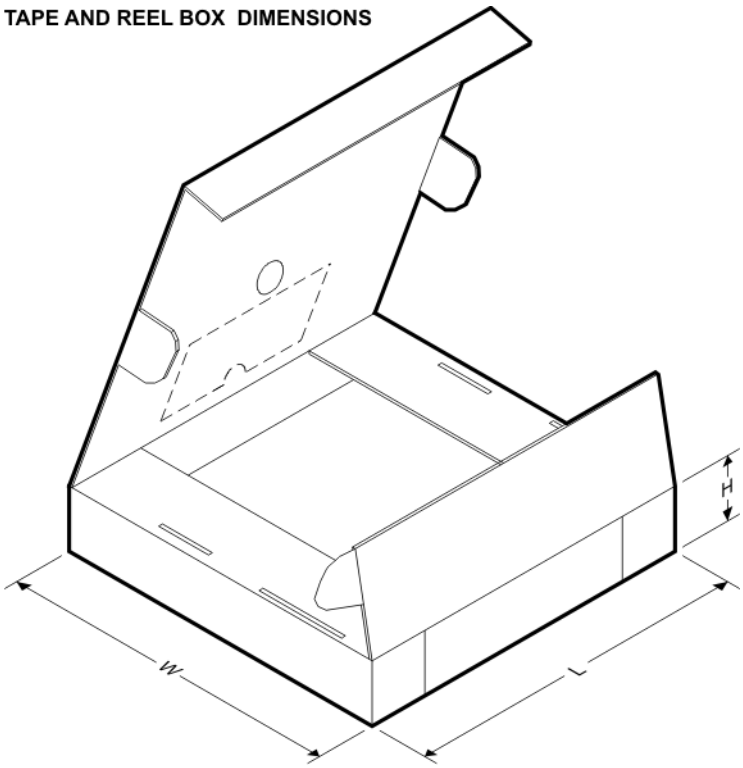
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4953SD/NOPB	WSON	NHK	14	1000	178.0	12.4	3.3	4.3	1.0	8.0	12.0	Q1
LM4953SDX/NOPB	WSON	NHK	14	4500	330.0	12.4	3.3	4.3	1.0	8.0	12.0	Q1

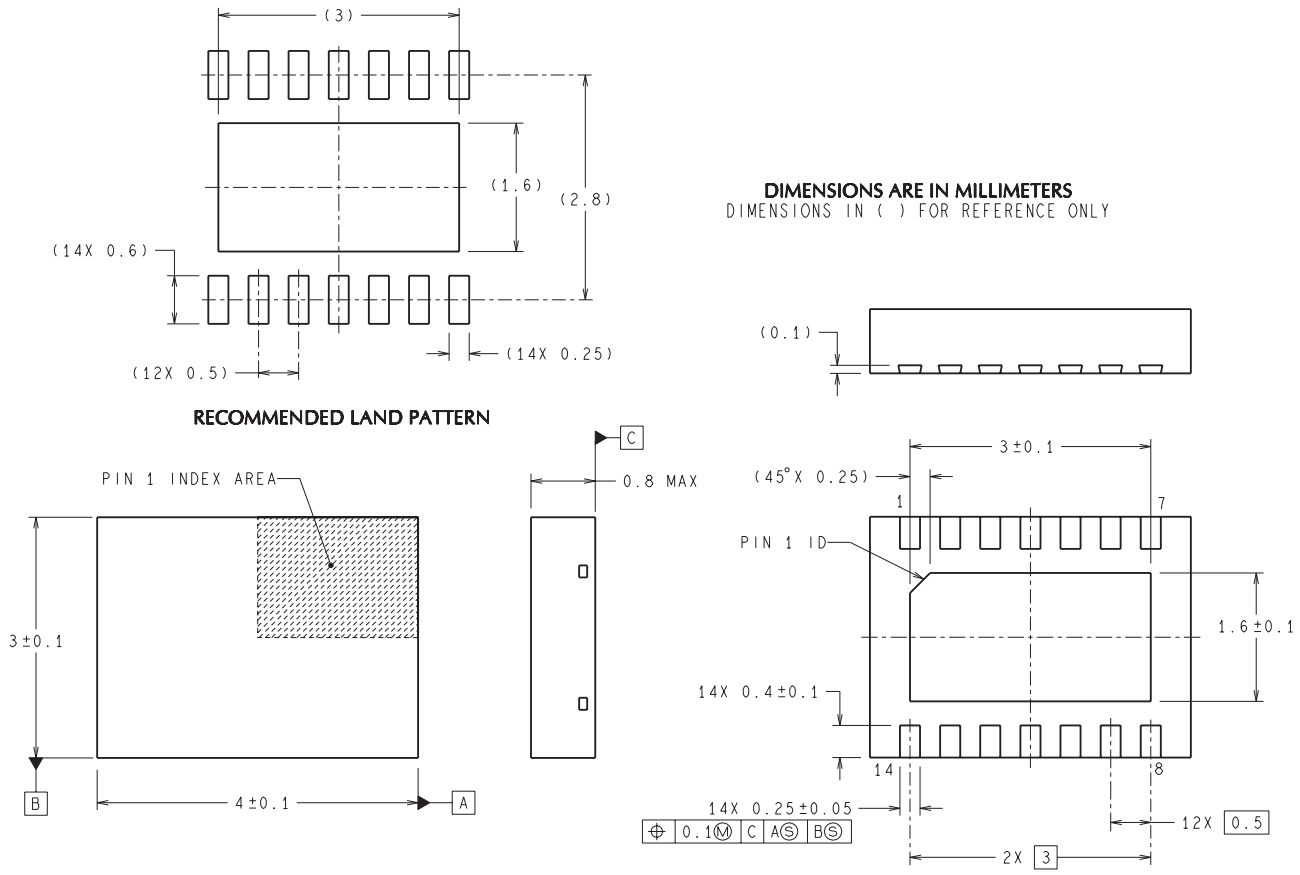
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4953SD/NOPB	WSON	NHK	14	1000	203.0	190.0	41.0
LM4953SDX/NOPB	WSON	NHK	14	4500	367.0	367.0	35.0

NHK0014A



SDA14A (Rev A)

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